

FIG. 1 (PRIOR ART)

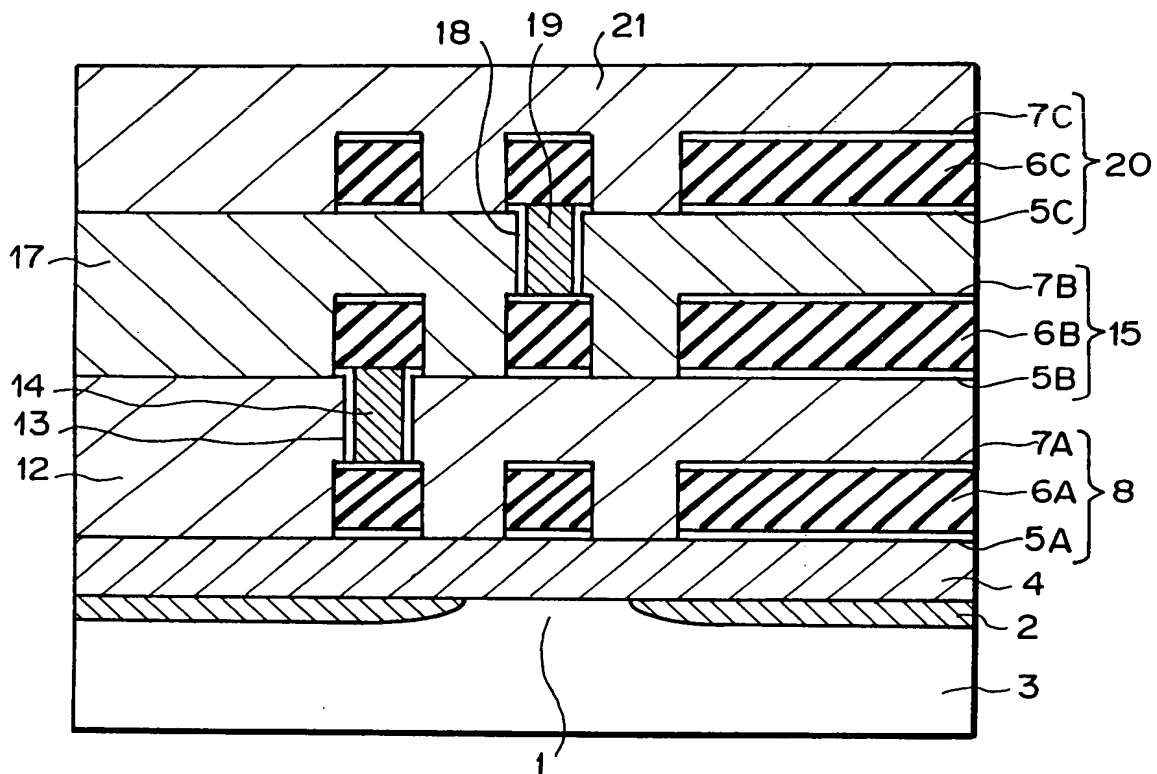


FIG. 2 (PRIOR ART)

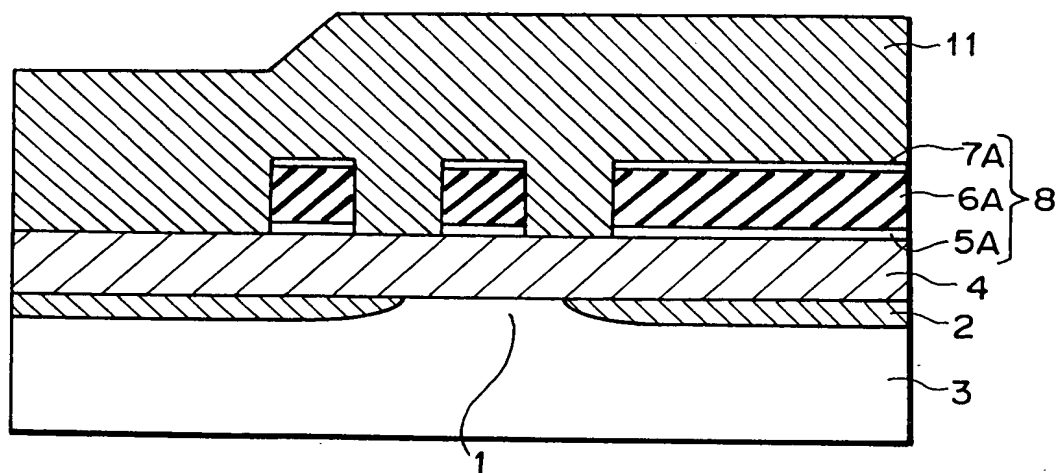


FIG. 3 (PRIOR ART)

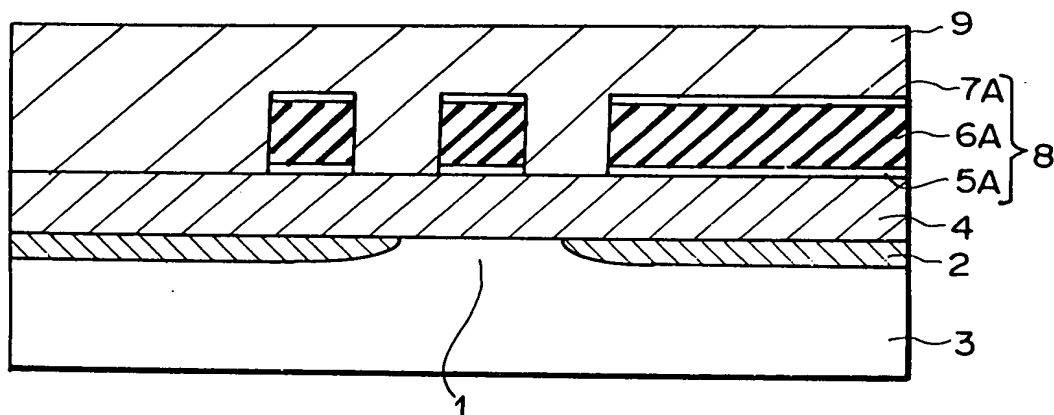


FIG. 4 (PRIOR ART)

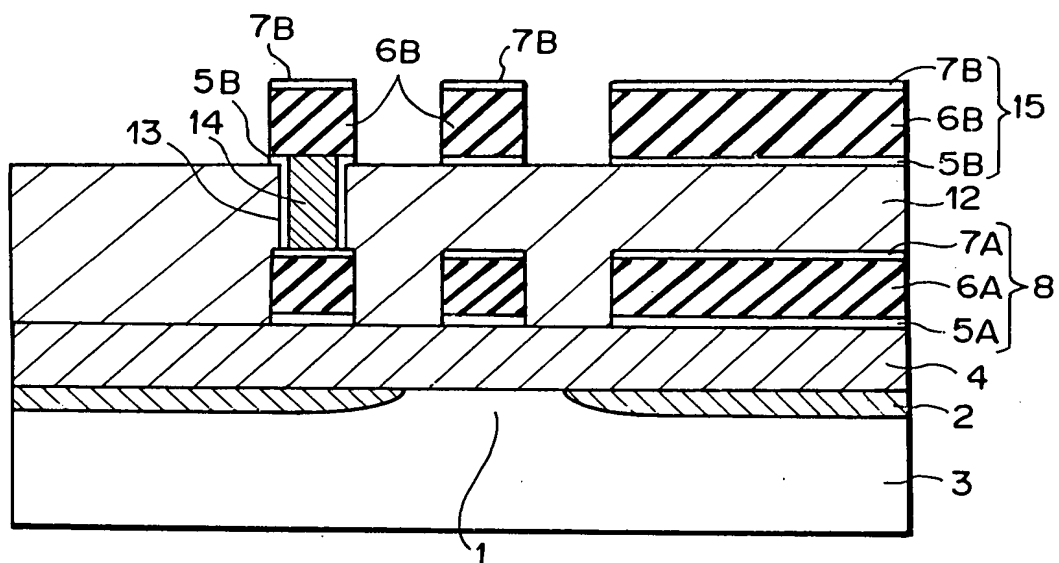


FIG. 5

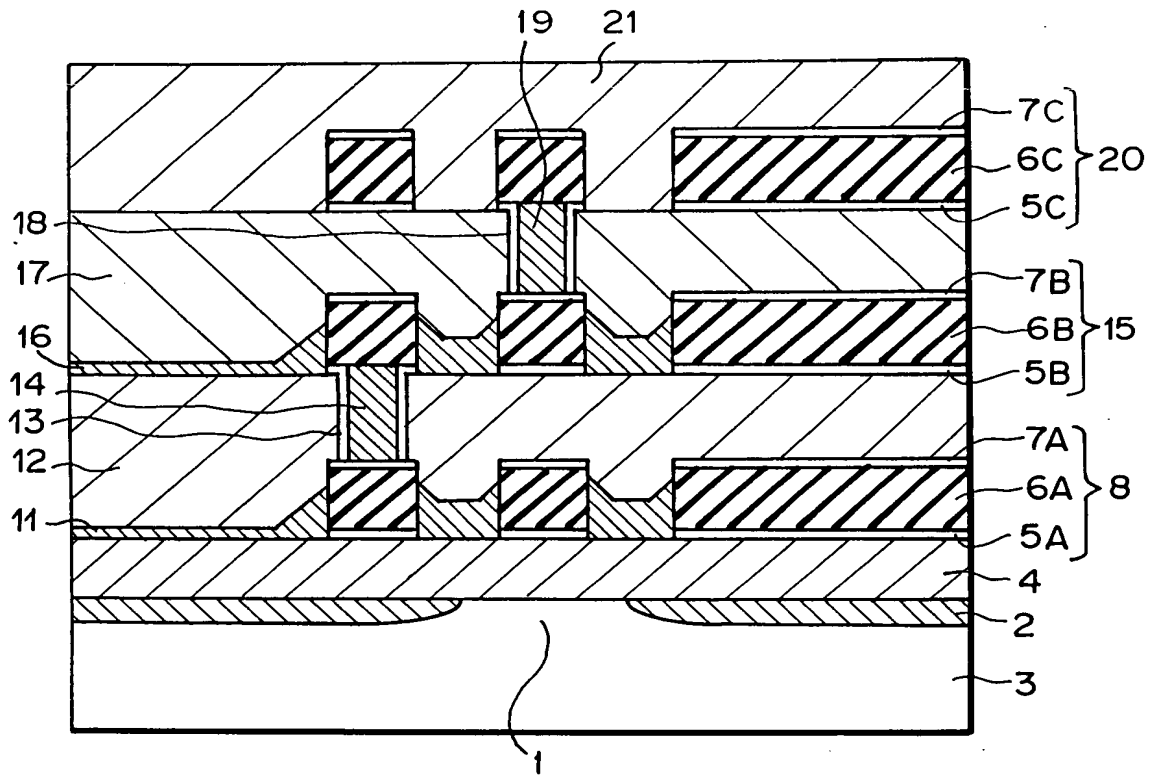


FIG. 6

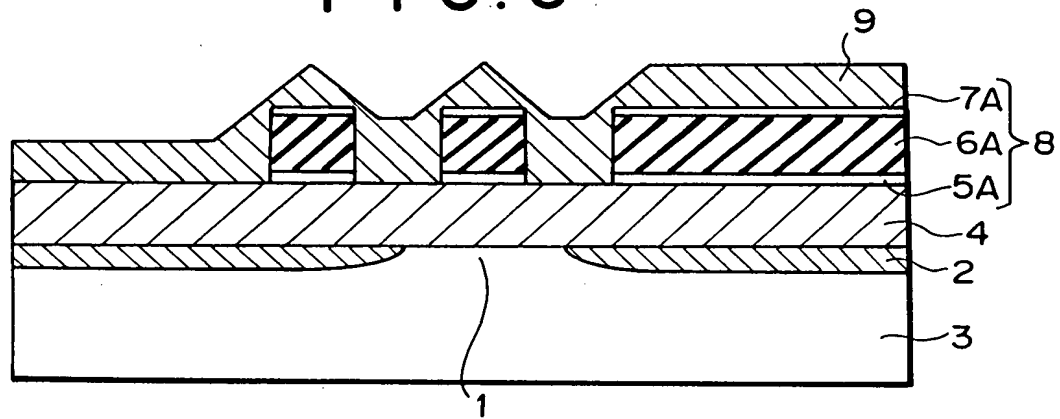


FIG. 7

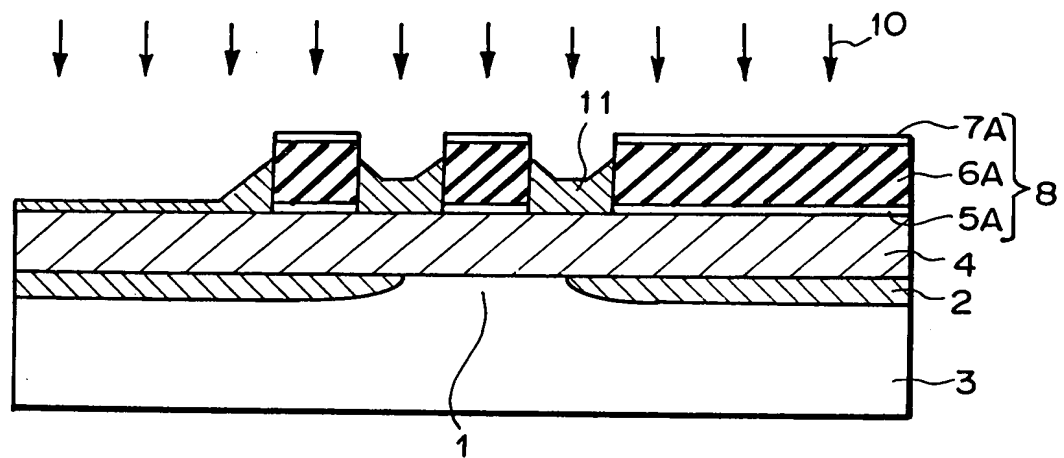


FIG. 8

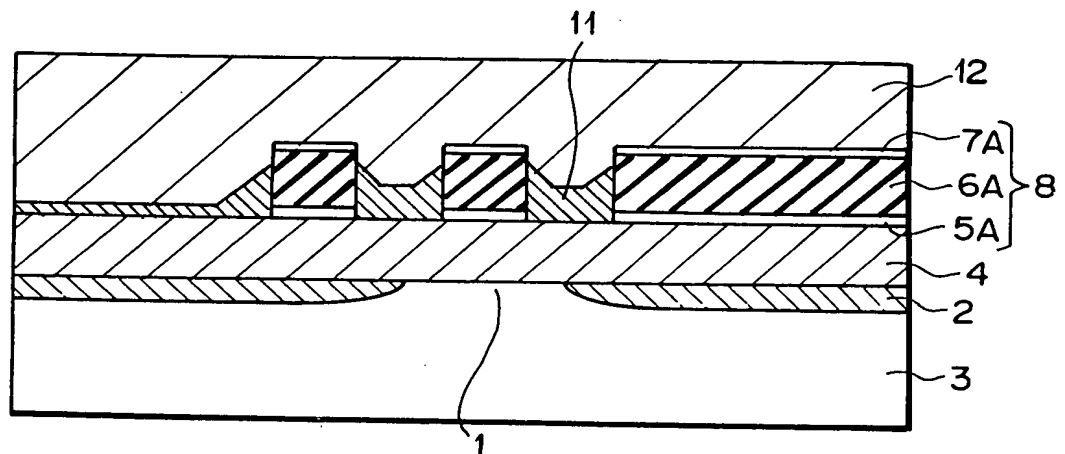


Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 1 with a thin layer 2, a thick layer 4, and a top layer 9. A central region 8 contains a patterned layer 5A with openings filled with material 6A, and a top layer 7A. The top layer 9 has a wavy profile.

A cross-sectional view of a semiconductor device. The device consists of a substrate 1 with a thin layer 2 on its top surface. Above layer 2 is a thick layer 4, which contains a thin layer 5A. On top of layer 4 is a patterned layer 8, which includes a layer 6A and a layer 7A. The patterned layer 8 is formed in a series of rectangular blocks. Above the patterned layer 8 is a thin layer 9. The top surface of the device is exposed to a series of downward arrows 10, representing incident light or a process step.

FIG. 10

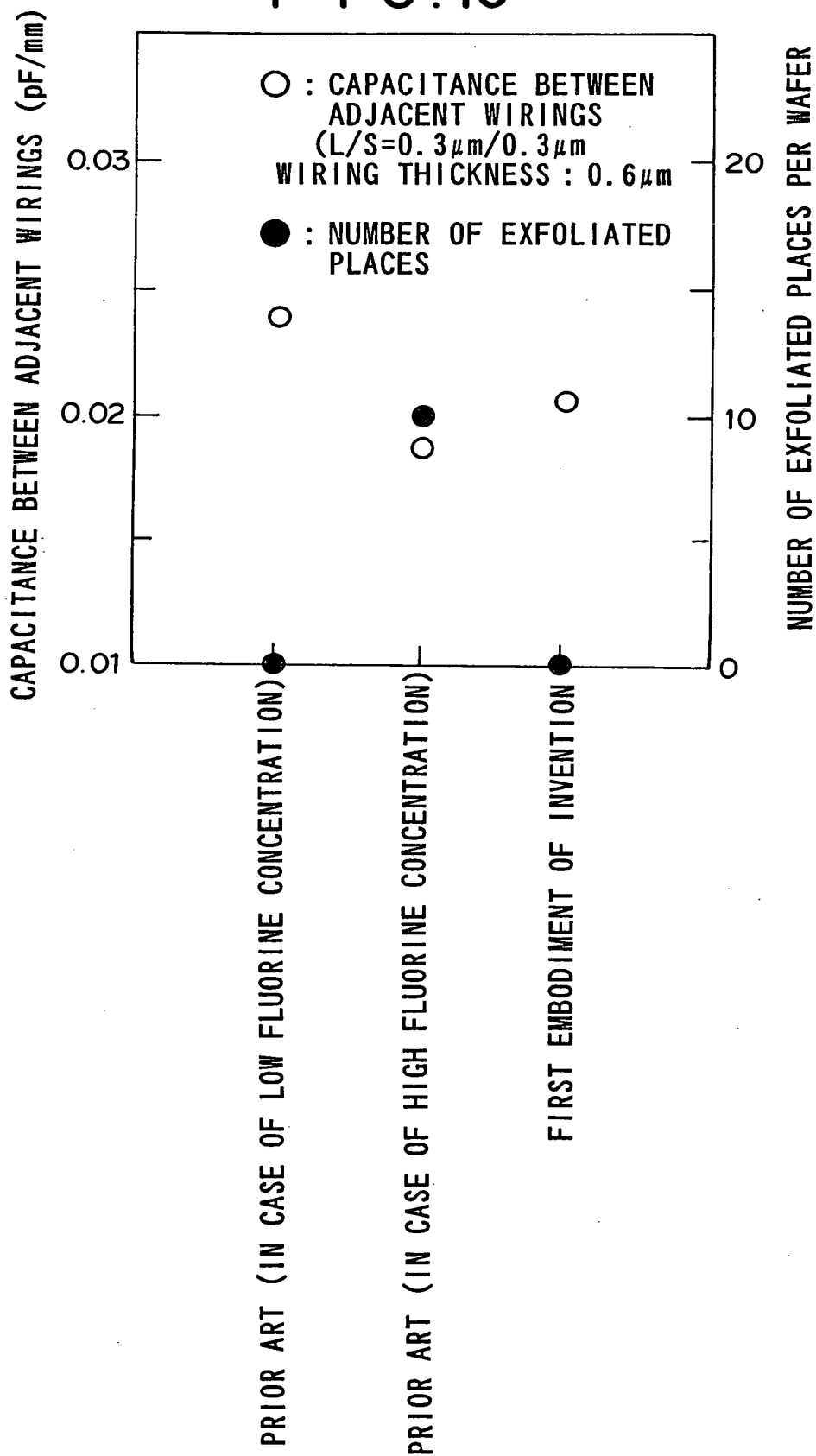


FIG. 13

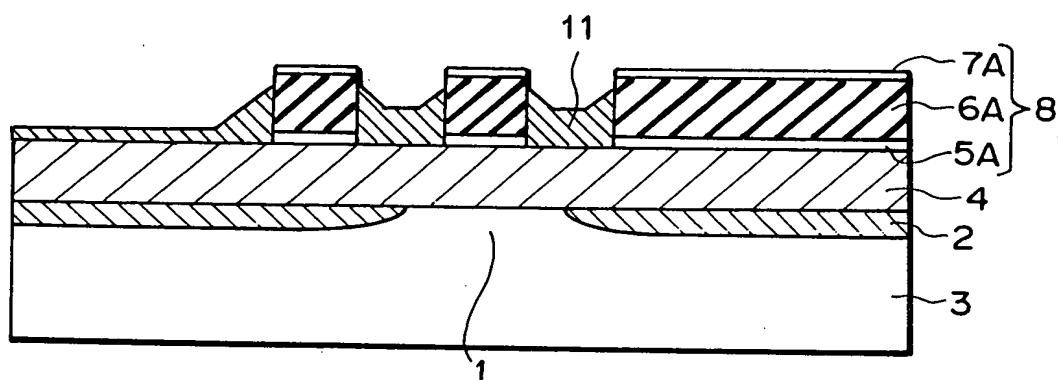


FIG. 14

